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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,757	07/31/2003	Larry J. Thayer	200313415-1	4651

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EXAMINER	
DARE, RYAN A	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,757	THAYER, LARRY J.	
	Examiner	Art Unit	
	Ryan Dare	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *July 31 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/31/2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/31/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

RD

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 112. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

1. Claim 4 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 4 discloses that the system hit signal is a logical OR of the row hit signals. Claim 1 discloses that the

system hit signal is a logical combination of the row hit signals wherein one or more of the row hit signals are high. This is the definition of logical OR, so claim 4 does not limit claim 1.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Khanna, US Patent 6,842,358.

4. With respect to claim 1, Khanna discloses a memory system, comprising:

A plurality of rows, in fig. 1, numeral 101,

each row receiving identical input bits, in fig. 1 numeral 111 and col. 1, lines 40-43,

each row having identical stored bits, in fig. 1, numeral 101,

each row generating, at a row output, a row hit signal when its stored bits match the input bits, in col. 1, lines 43-49,

and the row outputs are logically combined to generate a system hit signal when at least one of the rows generates a row hit signal, in fig. 1, MFLAG output and described in col. 1, lines 54-56.

5. With respect to claim 2, Khanna discloses the memory system of claim 1, where each row in the plurality of rows is in a different memory, in fig. 2 where primary array segment 221 is the first memory and the cascaded array segment 223 is the second memory.

6. With respect to claim 3, Khanna discloses the memory system of claim 1, where at least two of the rows in the plurality of rows are in one memory, in the embodiment of fig. 1, where there is only one memory.

7. With respect to claim 4, Khanna discloses the memory system of claim 1, where the system hit signal is a logical OR of the row hit signals, in col. 1, lines 54-56. Referring to fig. 1, the output of the FLAG circuit 107 will indicate whether one or more match was detected with the signal line MFLAG, and thus constitutes a logical OR.

8. Claims 5-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Regev, US Patent 6,707,694.

9. With respect to claim 5, Regev discloses a computer system, comprising:

a cache memory, in fig. 6, numeral 605; and

a content addressable memory associated with the cache memory, in fig. 6, numeral 608 and col. 6, lines 49-52,

the content addressable memory receiving input bits, in fig. 2, M0 through M7 and col. 1 lines 39-42,

the content addressable memory storing a plurality of copies of at least part of an address for each data item in the cache memory, in col. 1, lines 49-51,

the content addressable memory generating a signal indicating a match to the input bits when at least one of the plurality of copies of at least part of an address for each data item in the cache memory matches the input bits, in col. 1, lines 45-47.

10. With respect to claim 6, Regev discloses a method, comprising:

receiving, by a memory system, input bits, in fig. 2, col. 1 lines 39-42, with reference to fig. 2, M0 through M7;

comparing, by the memory system, the input bits to a plurality of identical sets of stored bits, in col. 1, lines 39-42; and

generating a signal indicating a match when at least one of the identical sets of stored bits matches the input bits, in col. 1, lines 49-51.

11. With respect to claim 7, Regev discloses a content addressable memory system, comprising:

means for storing a plurality of copies of stored bits, in fig. 2, and described in col. 1, lines 36-42;

means for comparing each copy of stored bits to input bits, in fig. 2, and described in col. 1, lines 39-42; and

means for generating a system hit signal when at least one of the plurality of copies of stored bits matches the input bits, in fig. 4, where the signal 408 is logical one when a match occurs. Also see col. 1, lines 49-51.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khanna, US Patent 6,842,358 and McCormick, Jr., US Patent 6,470,438.

14. With respect to claim 8, Khanna discloses a memory system, comprising:

A plurality of rows, in fig. 1, numeral 101,

each row receiving identical input bits, in fig. 1 numeral 111 and col. 1, lines 40-43,

each row having identical stored bits, in fig. 1, numeral 101,

each row generating, at a row output, a row hit signal when its stored bits match the input bits, in col. 1, lines 43-49,

Khanna fails to disclose that the output signal is the result of at least half of the signals from the row outputs.

McCormick, Jr. discloses a similar memory system wherein redundant copies of data are stored in an associative cache memory, where the system output signal is the logical combination of the row outputs, corresponding to at least half of the signals from the row outputs, in col. 3, lines 44-46.

15. It would have been obvious to one of ordinary skill in the art, having the teachings of Khana and McCormick, Jr. before him at the time the invention was made,

to combine the memory system of Khana with the memory system of McCormick, Jr., in order to reduce false hits as discussed by McCormick, Jr. in the abstract.

16. With respect to claim 9, Khanna and McCormick, Jr. disclose all limitations of the parent claim, as discussed supra, and also teach claim 9, where the row outputs are logically combined to generate a system output signal corresponding to a majority of the signals from the row outputs, in col. 3, lines 44-46.

Conclusion

17. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider these references fully when responding to this action. The documents cited therein teach similar systems of dealing with TLB invalidations.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Dare whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RD

Ryan Dare
September 28, 2005

MATTHEW D. ANDERSON
PRIMARY EXAMINER